FIG. 1A

PRIOR ART

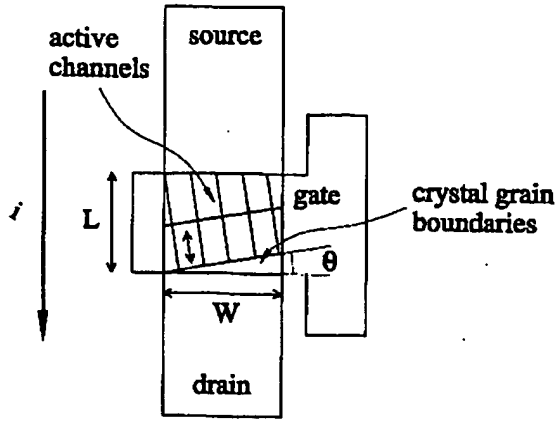


FIG. 1B

PRIOR ART

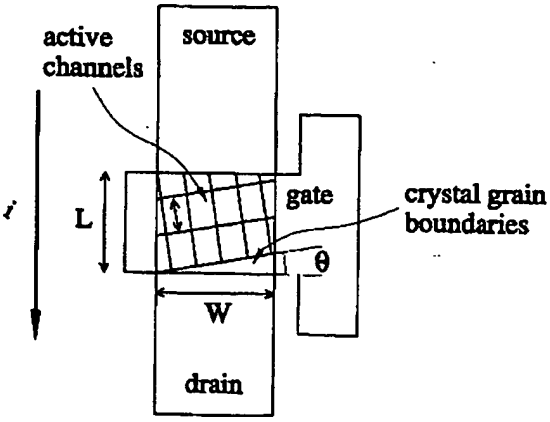


FIG. 2A

PRIOR ART

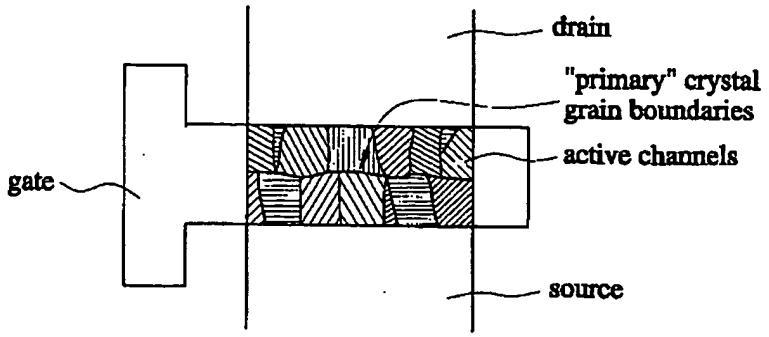


FIG. 2B

PRIOR ART

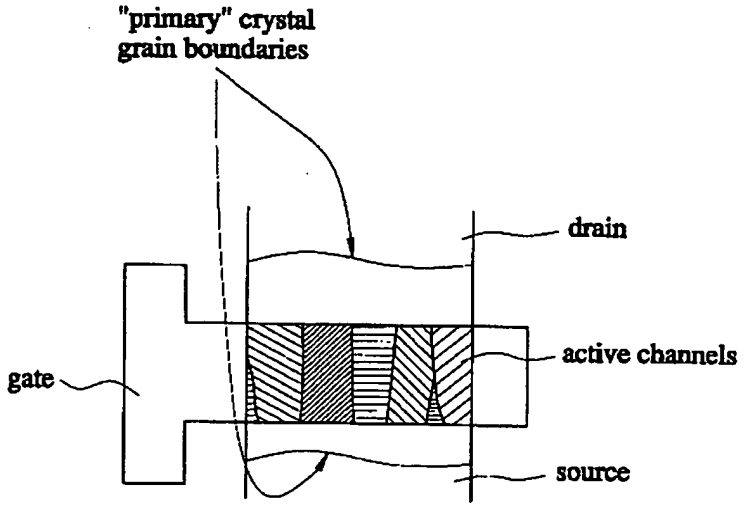


FIG. 3A

PRIOR ART

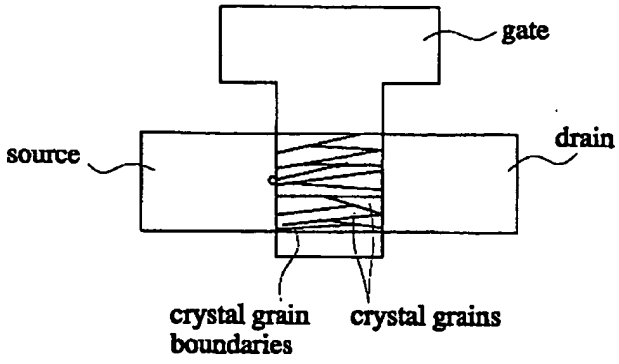


FIG. 3B

PRIOR ART

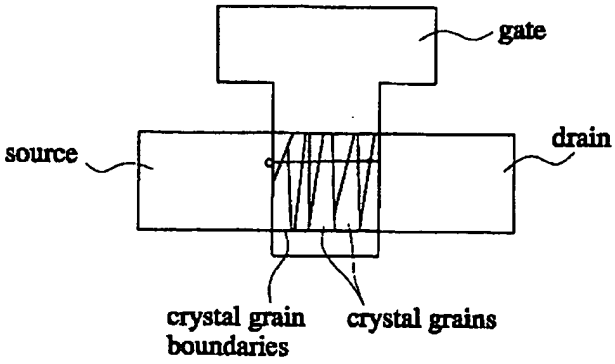


FIG. 3C
(PRIOR ART)

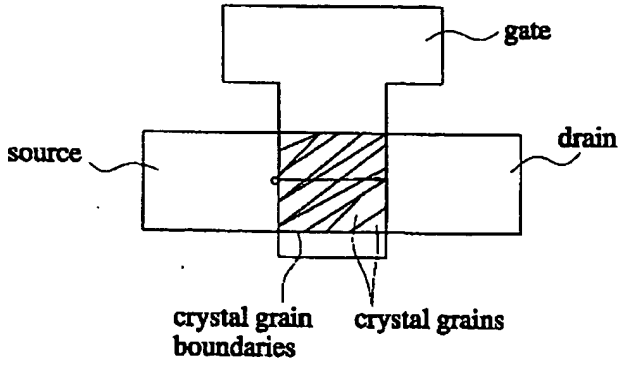


FIG. 4

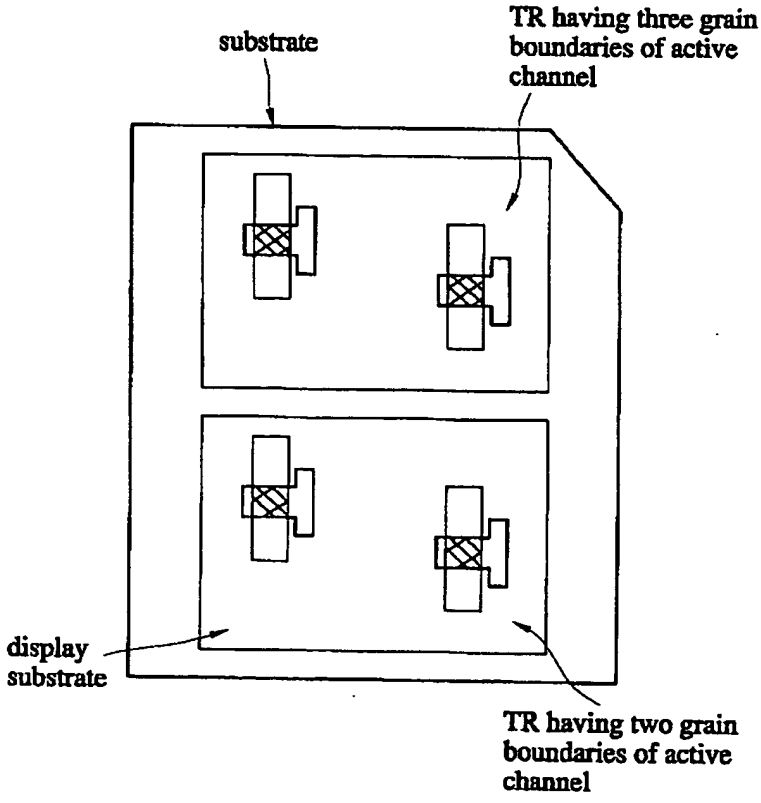

substrate
TR having three grain boundaries of active channel
display substrate
TR having two grain boundaries of active channel

FIG. 5A

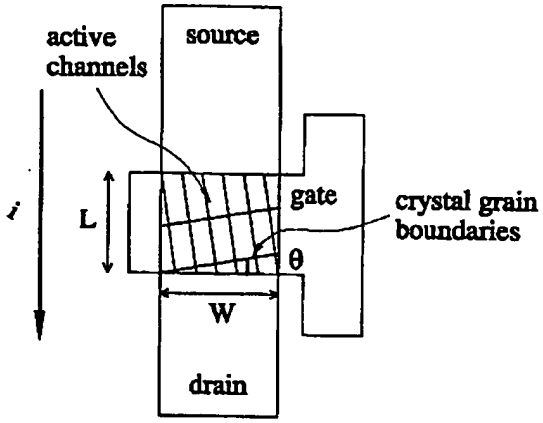

active
channels
source
gate
crystal grain
boundaries
L
θ
W
drain

FIG. 5B

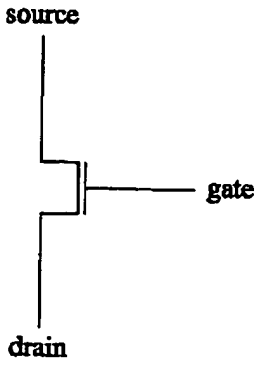

source
gate
drain

FIG. 5C

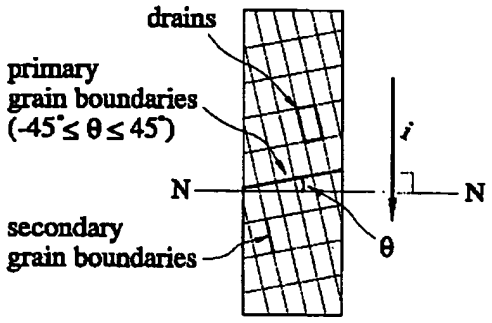

drains
primary
grain boundaries
(-45°≤ θ ≤ 45°)
N
N
secondary
grain boundaries
θ
i

FIG. 6A

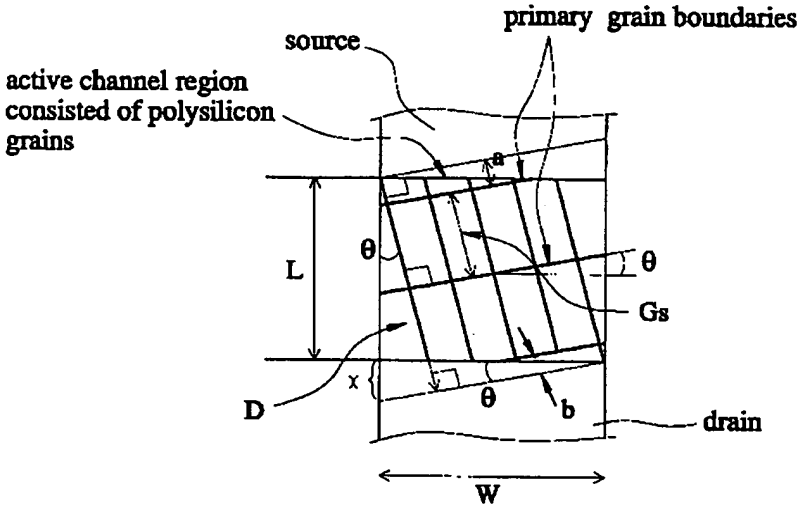

primary grain boundaries
source
active channel region
consisted of polysilicon
grains
a
L
θ
θ
Gs
x
D
θ
b
drain
W

FIG. 6B

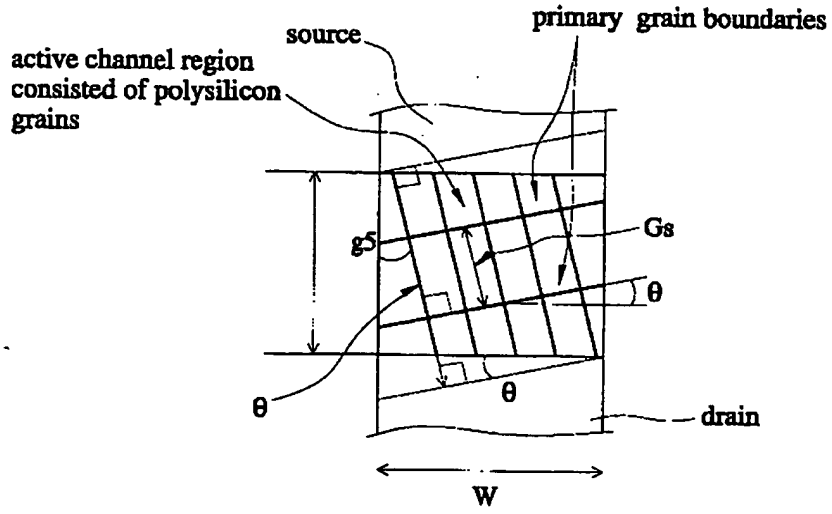

primary grain boundaries
source
active channel region
consisted of polysilicon
grains
g5
Gs
θ
θ
θ
drain
W

FIG. 7A

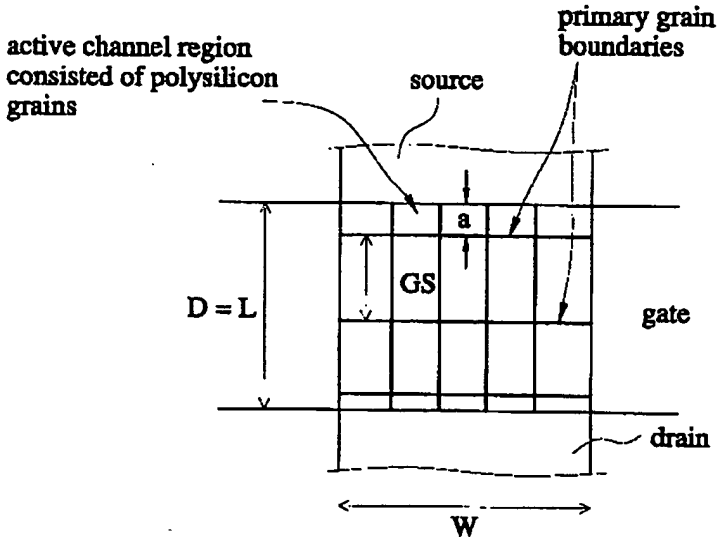

active channel region
consisted of polysilicon
grains
source
primary grain
boundaries
a
GS
D = L
gate
drain
W

FIG. 7B

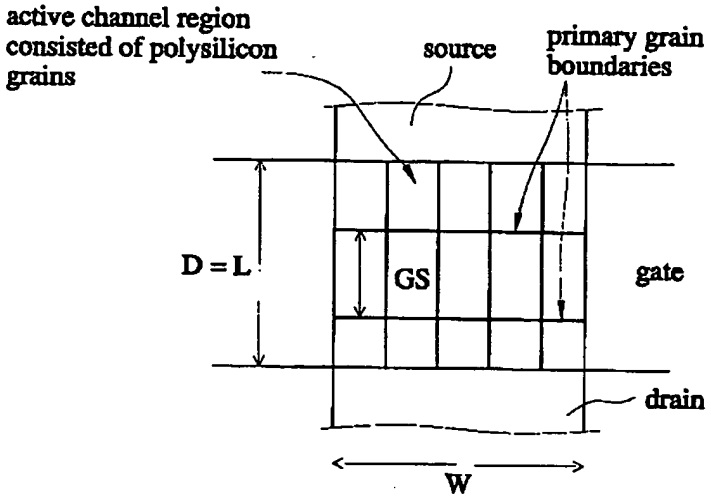

active channel region
consisted of polysilicon
grains
source
primary grain
boundaries
D = L
GS
gate
drain
W

FIG. 8A

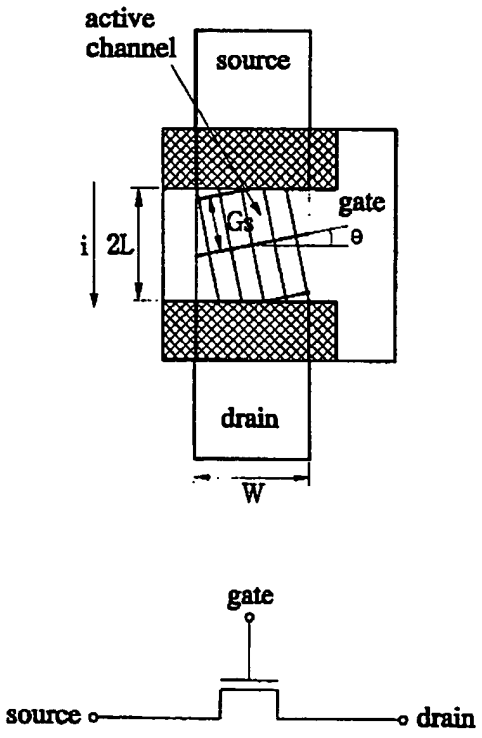
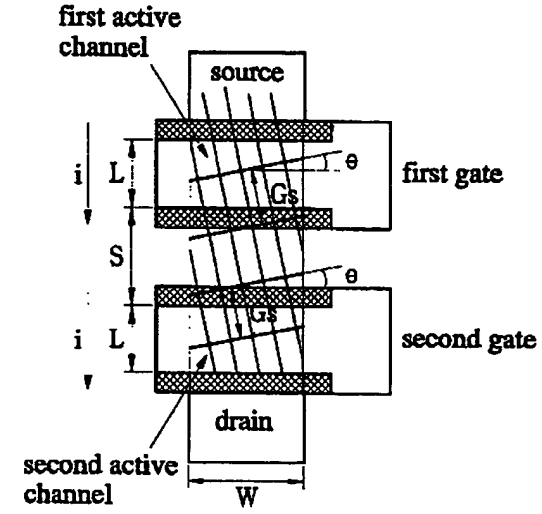

active
channel
source
gate
Gs
θ
i
2L
drain
W
gate
source
drain

FIG. 8B


first active channel
source
i
L
θ
first gate
Gs
S
θ
i
L
second gate
drain
second active channel
W

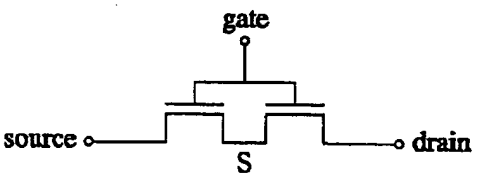

gate
source
drain
S

FIG. 9

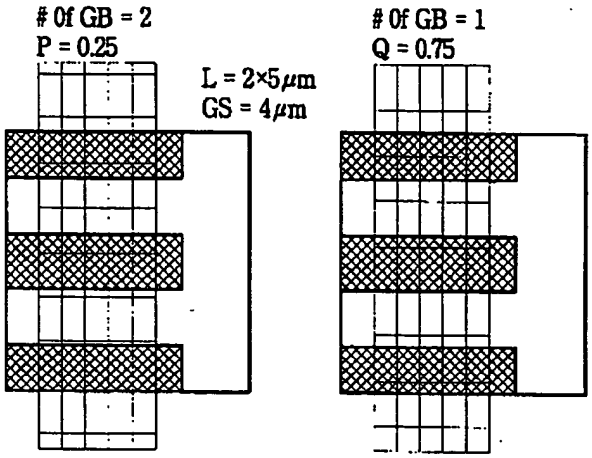
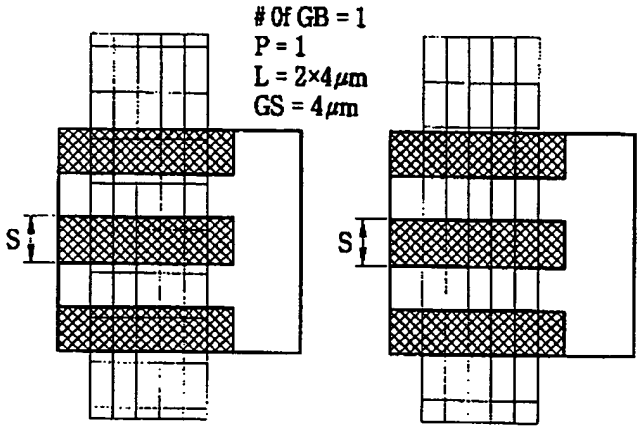



FIG. 10